



Zhone Technologies, Inc.

@Zhone Way
7001 Oakport Street
Oakland, CA 94621
Phone: 510.777.7000
Fax: 510.777.7001

www.zhone.com

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Subject: FAR 324: NOS Alarms on IMACS WAN circuits

Product: IMACS PRM-891130 WAN Daughter Board

Summary

A problem was reported on product performance issue on the IMACS wide area network (WAN) connections. It was found that some 81130 WAN digital signal cross connect (DSX) daughter boards may cause intermittent no signal (NOS) alarms on WAN circuits. The NOS alarms are sometimes accompanied by carrier group alarm red (CGA RED) or carrier group alarm yellow (CGA YELLOW) alarms on the IMACS at the opposite end of the circuit. Depending on the system's configuration, this may cause intermittent service interruptions to some or all services carried by the IMACS system.

Zhone found that the 81130 WAN Daughter boards were at times outputting a T1 signal outside specified T1 voltage range which is the root cause of the reported issue.

Background & History

The 81130 WAN Daughter board has been in production for many years with very low failure rates.

In February of 2006 the Crystal chip was used on the daughter board instead of the more commonly used Intel T1 Interface chip. The Crystal chip has always been listed as the second supplier part on the BOM for the 81130 daughter board. Since the Crystal chip is the second part on the BOM it can be substituted at any time. The Crystal chip has been used in the past without causing any failures in manufacturing test, or any failures reported in the field. We do not track the Authorized Vendor List (AVL) components against the board serial number and are unable to tell which boards in the field have which interface chip. Since there have been no reported field failures until this year, and since manufacturing has never noted a problem with the boards with the Crystal chip, we believe the previous chips were working in an acceptable range and have not caused NOS issues in the field as recently seen by the field.



It was noticed that the boards built with the Crystal chips during the months of February and March were having a higher than normal failure rate than the boards built with the Intel Chips, and boards previously built with Crystal chips. At this time (March 2006) manufacturing was instructed to stop building boards with the Crystal chips.

The boards that were sent to the field passed systems test and appeared to be operating normally. It was only in the field environment, and then intermittently, that the problems became apparent.

Root Cause:

Some 81130s output an “out of specification” DS1 or E1 signal. The specification for a DS1/E1 signal is 7.2 volts peak to peak maximum. The problematic 81130s may intermittently exceed the 7.2 volt peak to peak limit. The out of range voltage on the DS1 may cause NOS alarms. It has been further determined that this problem exists only on certain 81130 DSX modules that were manufactured by Zhone with an integrated circuit (chip) that was manufactured by Cirrus and branded with the “Crystal” logo. These modules may also have been manufactured with Intel manufactured chips which are branded with either the “Intel” or “Level One” logo.

Corrective Action:

The manufacturing test criteria for the 81130 have been tightened to eliminate this potential problem from reaching the field. The test previously passed cards that were within the 4.8 to 7.2 volts peak to peak range. The new test criteria only allows cards within the range of 5.0 to 7.0 volts peak to peak. This will allow for any variance in the T1 interface chip.

We currently have stopped manufacturing any new boards with the Cirrus Crystal chip. Manufacturing has found a large supply of Intel interface chips and will use this as long as possible.

Engineering has provided an Engineering Change Order (ECO) (11251) that will correct the output level of the 81130 with the Crystal chip. Manufacturing has instructions to only implement this ECO if and when we find that the Intel interface chip is no longer available. The ECO changes the output value of the 81130 to the nominal peak to peak value of 6.0 volts with the Crystal chips on board.

Conclusion:

This problem has been eliminated by currently using only Intel T1 interface chips on the 81130 daughter board and by tightening of the test specification of the board.

In the future if Crystal chips must be used ECO 11251 will be implemented to accommodate for the higher output level of the Crystal chip.



Field returns with the Crystal chip will have the above ECO implemented on them and they will be returned to class B stock.

Jim Hughes
Q.A. Engineer
Zhone Technologies, Inc.